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**FILING DATE:** *October 31, 2003*

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Docket No. 212/541

# Provisional Application for Patent Cover Sheet



To: MS Provisional Patent Application
Commissioner for Patents
P.O. Box 1450
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Sir: Enclosed for filing please find the following provisional patent application:

Title: Nano-contacted Magnetic Memory Device and Method For Making Same

Enclosed please also find the following papers:

Serial Number:

☒ 12 pages Specification; 1 pages claims; 1 pages abstract

Filing Date October 31, 2003

☒ 12 sheets of drawings

☐ Power of Attorney

☐ Assignment of the invention

☐ A Verified Statement Claiming Small Entity Status

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Post Office Address:

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Residence: Citizenship
Post Office Address:

☐ Applicant claims small entity status.

The provisional application filing fee of $160 is due.

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Niky Economy Syrengelas, Esq.

# Nano-contacted Magnetic memory device and method for making same

## FIELD OF THE INVENTION

The present invention relates to a magnetic memory device. In particular, it relates to a magnetoresistive random access memory (MRAM) device with current-perpendicular-to-plane (CPP) MRAM cells that write data by thermal assisted techniques.

## BACKGROUND OF THE INVENTION

Memory devices are used in a wide variety of applications. Such applications include personal computers, consumer products such as digital cameras, digital video cameras and mobile phones. There are many different memory devices. The type of memory devices chosen for a specific function depends largely upon what features of these devices are best suited to perform that specific function. For instance, volatile memories, such as dynamic random access memories (DRAMs) must be continually powered in order to retain their contents. However, DRAMs tend to provide greater storage capability and programming option and cycle than non-volatile memories such as read only memories (ROMs). Efforts have been underway to create a commercially viable memory device that is both random access and non-volatile. Ovshinsky et al disclosed a phase changed memory or chalcogenide random access memory (CRAM), which includes a chalcogenide material or phase change material, in US patent 5,296,716. The phase change material can be electrically switched between generally amorphous and generally crystalline states. However, the fatigue property is a key issue in CRAM due to high temperature heating. The cell uniformity in products is also a key issue due to the reading method. Since the cell resistance is detected during reading, any non-uniform cell resistance generates an

error. Magnetoresistive random access memory (MRAM) device disclosed by Daughton James M in US. patent 4,731,757 and US. patent 6,021,065 is another type of solid state, non-volatile memory device. A conventional MRAM device includes a column of first electrical wires, referred to as "word lines", and a row of second electrical wires, referred to as "bit lines". An array of memory cells located at junctions of the word lines and bit lines, is used to record data signals.

A typical memory cell of MRAM comprises a magnetoresistive element, wherein the magnetoresistive element comprises a hard magnetic layer, a soft magnetic layer, and a non-magnetic layer sandwiched between the hard magnetic layer and the soft magnetic layer. The hard magnetic layer has its magnetization vector fixed in one direction. The orientation of the fixed magnetization vectors does not change under a magnetic field applied thereon. The soft magnetic layer has an alterable magnetization vector, under a magnetic field applied thereon, that either points to the same direction, hereinafter "parallel alignment", or opposite direction, hereinafter "anti-parallel alignment", of the magnetization vector of the hard magnetic layer. Since the resistances of the magnetoresistive element in the "parallel alignment" status and the "anti-parallel alignment" status are different, the two types of alignment status can be used to record two logical states – the "0"s or "1"s of a data bit.

In a write operation, an electric current passes through the word line and the bit line adjacent to a memory cell. When the electric current reaches a certain threshold, the magnetic field generated by the electric current switches the orientation of the magnetization vector of the soft magnetic layer in the magnetoresistive element. As a result, magnetization of the hard magnetic layer and the soft magnetic layer changes from one type of alignment, e.g. "parallel alignment", to the other type of alignment, e.g. "anti-parallel alignment", so that a data signal can be recorded in the memory cell.

In order to increase the thermal stability of a memory cell, a Curie point written MRAM has been proposed to improve the MRAM stability, as described in US patent

6,535,416 to Daughton James M. et al, , and in a paper by R.S. Beech et al titled "Curie point written magnetoresistive memory", J.Appl. Phys. 87, No. 9, 6403-6405, 2000. A Curie point written structure has been disclosed in these structures, where a single pinned layer is used as storage layer. The pinned layer has a higher anisotropy than a soft layer that is not pinned by another layer. The use of the pinned layer for information storage provides improved thermal stability and allowing the size of a memory cell to be further reduced before thermal instability becomes a limiting factor.

In order to increase the density of MRAM, one can simplify the MRAM structure as mentioned in US Patent 6,597,618 B2, US Patent 6,341,084 B2, US Patent 6,317,375 B1 and US patent 6,259,644 B1.

Most MRAMs use a vertical structure or current-perpendicular-to-plane (CPP) structure due to their high density integrated with semiconductor device. The CPP structure includes magnetic tunnel junction (MTJ) and CPP spin-valve, both are magnetoresistive element. Generally, an MTJ comprises a ferromagnetic free layer such as CoFe, an insulator layer such as AlO, a ferromagnetic pinned layer such as CoFe, and an anti-ferromagnetic pinning layer. As the size of a memory cell scales down to sub-100 nm, a thin insulator layer less than 1 nm is required to reduce the resistance of the MTJ. As the insulator layer gets thinner, the resistance uniformity of the MTJ deteriorates. A typical CPP spin-valve comprises a ferromagnetic free layer such as CoFe, a metal space layer such as Cu, a ferromagnetic pinned layer such as CoFe, and an anti-ferromagnetic pinning layer. As mentioned above, the uniformity of the resistance of the CPP spin-valve is a key issue. One solution is to detect the magnetization state of the ferromagnetic pinned layer by changing the magnetization state of the ferromagnetic free layer during a read operation. The non-uniformity issue can be overcome by detecting the resistance change. However, as the size of the MTJ or CPP spin-valve scales down, an increased read power is required to switch the smaller cell.

## SUMMARY OF THE INVENTION

In one aspect of the invention, the invention relates to a high density and low cost MRAM unit comprising:

a substrate;

a plurality of switch transistors formed on the substrate;

a plurality of memory blocks, each of the plurality of memory blocks having a recording layer and a plurality of active areas associated therewith;

a plurality of contacts, each of the plurality of contacts being to couple an electrode of each of the plurality of switch transistors to an active area of each of the plurality of memory blocks;

a bit line and a word line in electrical contact with the plurality of switch transistors; and

a digital line formed under or above the memory blocks,

wherein each of the plurality of switch transistors is controllable to activate a respective contact and thereby write onto the recording layer at a respective active area.

In a preferred embodiment of the invention, the memory blocks comprises a recording layer, a space layer, and a reading layer. The recording layer comprises an anti-ferromagnetic (AFM) layer, a first ferromagnetic layer, a first space layer, and a second ferromagnetic layer. The first ferromagnetic layer is pinned through the AFM layer. And the first and second ferromagnetic layers are coupled anti-ferromagnetically. Each of the two ferromagnetic layers has a fixed magnetization vector. Thus the AFM layer and the two ferromagnetic layers form the synthetic-anti-ferromagnetic-pinned (SAFP) recording layer. The reading layer is a free layer that can be a soft magnetic layer. The magnetization of the free layer at the memory block can be changed during a read operation. Since the memory block can be much larger than an active area, there is no requirement of fine patterning of a magnetoresistive element that is of a size of an active area.

The recording layer near a contact can be recorded by means of thermal assistant writing,

wherein a heat element adjacent to an active area of each of the plurality of memory block heats the recording layer of the memory block at the active area to a temperature near to the Blocking point of the recording layer, independent from other active area, and

the magnetization vector of the recording layer at the active area is aligned with a magnetic field generated by a current applied to a digital line and a bit line or word line.

In another preferred embodiment of the invention the plurality of memory blocks is a plurality of stacked structure including current-perpendicular-to-plane (CPP) structure such as magnetic tunnel junction (MTJ) and CPP spin-valve (SV).

In another aspect of the invention, there is provided a method of writing data to a MRAM unit comprising a plurality of switch transistors, a plurality of memory blocks, and a plurality of heat elements adjacent to a respective active area of each of the plurality of memory block, the method including the steps of:

raising the temperature of a recording layer at an active area of the plurality of memory block to a temperature near to the Blocking point of the recording layer, independent from other active area, thereby reducing the coercivity of the recording layer at the respective active area;

altering the magnetization state of the recording layer at the active area by passing a current through a digital line and a bit line or word line; and

the current in the digital line and the bit line or the word line acting cooperatively to align the magnetization state of the recording layer with a magnetic field generated by the current.

The size of the plurality of memory blocks depends upon many factors, such as the heating current, size of the contact, the total thickness of the plurality of memory blocks, magnetic field generated by the digital line and the word line or the bit line, etc.

In yet another aspect of the invention, there is provided a method of performing a read operation in a MRAM unit comprising a plurality of switch transistors and a plurality of memory blocks, the method including the steps of:

applying a voltage on a word line to open a transistor;

applying a current through a bit line to sense the resistance of an active area of the plurality of memory block;

applying a current through a digital line to change the magnetization of afree layer in the plurality of memory blocks; and

determining the magnetization state of a recording layer in the plurality of memory blocks,

wherein the resistance of the active area is dependent on the relative angles between the magnetization vectors of the recording layer and free layers.

The resistance of the active area representing the magnetization states of the MRAM, and a read data is represented by the magnetization states stored in the active area of the plurality of memory blocks.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a 6F^2 DRAM cells layout (top view);

Fig. 1B is an equivalent circuit of a DRAM cell;

Fig. 1C is a cross section of a DRAM cell;

Fig. 2A is an equivalent circuit of a CPP type MRAM cell with a transistor;

Fig. 2B is a cross section of the CPP type MRAM cell with a transistor;

Fig. 2C is an enlarged view showing a magnetoresistive element of the CPP type MRAM cell shown in Fig. 2A;

Fig. 3A is a cross section showing a MRAM with CPP magnetoresistive element such as MTJ and CPP SV according to one embodiment of the present invention;

Fig. 3B is an equivalent circuit of the MRAM shown in Fig. 3A;

Fig. 3C is a different view of the MRAM shown in Fig. 3A;

Fig. 4A and 4B show the detailed writing process;

Fig. 5A and 5B show the voltage potential and current density distribution for a CPP type MRAM cell after applying a voltage on the contact hole;

Fig. 6A and 6B show the voltage potential and current density distribution for one CPP type MRAM cell after considering of the neighbor contact hole;

Fig. 7 shows the conductance dependence on the width of memory block with different thickness or space between the contact and electrode;

Fig. 8A and 8B show the typical MR-H curve after thermal assistant writing;

Fig. 8C and 8D show the magnetization states for a MRAM cell after thermal assistant writing;

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1A shows a 6F^2 DRAM cells layout (top view). The DRAM includes vertical bit lines 10, horizontal word lines 12, capacitor contacts 14, bit line contacts 16, and active (diffusion) areas 18 that include a source region and a drain region. The word lines contact with a gate electrodes and the bit lines contact with the source region. The capacitor contacts are located between the capacitor and the drain region. Fig. 1B shows an equivalent circuit of a DRAM cell. Capacitor 20 is connected with the drain of a transistor 21. Word line 23 is connected with the gate of the transistor 21. And bit line 22 is connected with the source of the transistor 21. Fig. 1C shows a cross section of a DRAM cell. Word line 37 is connected with the gate 34 of a transistor 31. Data line 36 is connected with the drain 32 of the transistor 31. A capacitor 35 is connected with the source 33 of the transistor 31 through a contact. Here the capacitor can be a stacked capacitor or a trench capacitor in order to increase the capacity.

Fig. 2A shows an equivalent circuit of a typical CPP type MRAM cell with a transistor 201. A bit line 203 is connected with the drain of the transistor 201 through

a magnetoresistive element 202. A Word line is connected with the gate of the transistor 201. A digital line 205 crosses the magnetoresistive element 205. Fig. 2B shows a cross section of a CPP type MRAM cell with a transistor. The source 211, a gate 212, and a drain 213 of a transistor are formed on a substrate 210. A digital line 214 is burned under a magnetoresistive element 215. The magnetoresistive element is connected with a bit line 216. The magnetoresistive element 215 comprises a template layer 220, a first free layer 221, a first non-magnetic layer 222; a first ferromagnetic layer 223, a second non-magnetic layer 224, a second ferromagnetic layer 225, an AFM layer 226, and a cap layer 227. The above layers are disposed in sequence as shown in Fig. 2C. The magnetization 228 of the free layer can be changed during a write process and the magnetization 229 of the pinned layer is fixed.

Fig. 3A is a cross section showing a MRAM with CPP magnetoresistive element such as MTJ and CPP SV according to one embodiment of the present invention. A transistor 316 with source 301, gate 302, drain 303 is formed on a substrate 300. Another Transistor 317 with source 304, gate 305, and drain 306 is also formed on the substrate 300. More transistors can be formed on the substrate, only two transistors are shown here for simplicity. Word line 307 is connected with the gate 302 and 305. Bit lines 309 and 311 are connected with drain 303 and 306 respectively. A Memory block 312 is formed above the transistors 316 and 317. The memory block 312 is connected with the transistors 316 and 317 through contacts 308 and 310 at respective active areas of the memory block 312. Effective magnetoresistive elements 318 and 319 are formed at the respective active areas of the memory block. More effective magnetoresistive elements can be formed after considering more transistors. One contact represents one effective magnetoresistive element. An electrode 313 is formed after the memory block 312. The electrode 313 can be a protective layer of the memory block 312 and patterned simultaneously with the memory block 312. The size of the memory block depends on the size and number of contacts and the layer structure of the memory block. A common

electrode 314 is connected with the memory block 312 through the electrode 313. A digital line 315 is formed above the electrode 314. As the effective magnetoresistive elements 318 and 319 are not confined by a physical barrier since they are formed on the same memory block 312, the current pass through the effective magnetoresistive elements is not completely perpendicular to the plane of the memory block 312, and shunting effect should be considered. The equivalent circuit of the MRAM is shown in Fig. 3B. Resistors 320 and 324 are effective resistors, and the resistors 322 and 325 are additional resistors that take into account of the shunting effect. Fig. 3C is a different view showing the MRAM in Fig. 3A. The digital line 340 is at the bottom of the common electrode 341, memory block 343 and electrode 342 are on top of the common electrode 341. The memory block 343 is connected to bit lines 348 and 349 through contacts and transistors. The gate of the transistors are connected to word lines 346 and 347. Four contacts 345 are shown in Fig.3C for illustration purpose only, but it should not limit the number of contacts that can be formed on the memory block 343. Here, the contact 345 serves as a probe, which only detect the resistance of the effective magnetoresistive element near the contact. The current density is confined in a very small area in the memory block 343.

Detailed writing process is shown in Fig. 4A and 4B. Contact 403 connects to memory block 410 at an active area forming an effective magnetoresistive element 409. Contact 403 serves as a write/read head for the effective magnetoresistive element 409. Pinned layer 402 is a recording layer in memory block 410. Free layer 401 is a reading layer in memory block 410. Electrode 404 contacts the free layer 401. Separated digital line 405 serves as write line, which switches the magnetization vector of the recording layer in the effective magnetoresistive element 409 during a write process, and as read line, which switches the magnetization vector of the reading layer in the effective magnetoresistive element 409 during a read process. For instance, when a current pulse 408 is applied through the contact 403, the current pulse 408 can heat the effective magnetoresistive element 409. After heating the recording layer to a temperature above its Blocking temperature, a current 406A,

which has a direction toward inside, introduces a magnetic field with positive direction to align the magnetization 407A of the recording layer at the effective magnetoresistive element 409 to a direction as shown in Fig. 4A. The current pulse 408 is then removed and the effective magnetoresistive element 409 cools down, the magnetization 407A remains as shown in Fig. 4A. However, after heating, a current 406B, which has a direction toward outside, introduces a magnetic field with negative direction to switch the magnetization 407B at the effective magnetoresistive element 409 to a direction as shown in Fig. 4B. After cooling down, the magnetization 407B remains as shown in Fig. 4B. In order to obtain a recording area or a effective magnetoresistive element as small as possible, current applied through the film should be well confined to minimize shunting effect, and material with a large anisotropy energy is required as recording layer in order to reduce transient parameter. Soft ferromagnetic layer is not suitable to serve as the recording layer due to large transient parameter. Ferromagnetic material pinned by an anti-ferromagnetic material is suitable as recording layer. When the temperature rises to the Blocking temperature of the recording layer, the magnetization of the recording layer can be easily switched, and the magnetization state can be maintained once the recording layer is cooled down. A synthetic-anti-ferromagnetic-pinned (SAFP) multi-layer is more preferred as recording layer due to the high thermal stability and high heating tolerance of the SAFP multi-layer. In the SAFP multi-layer, two ferromagnetic layers are anti-ferromagnetically coupled, and they are pinned by an anti-ferromagnetic material. In order to improve the thermal stability, more anti-ferroamgnetically coupled ferromagnetic layers can be used in the SAFP multi-layer. As the coercivity of a ferri-magnetic materials reduces rapidly when the temperature rises to the Curie point, ferri-magnetic materials such as TbFeCo, DyFeCo and their alloys are also good candidates of the recoding layer. Generally, any ferromagnetic material can be used as the recording layer.

One issue in the proposed MRAM is how to confine the current in the effective magnetoresistive elements. Fig. 5A and 5B shows the voltage potential and current

density distribution for a CPP type MRAM cell after applying a voltage on a contact respectively. Here, the contact dimension is 100nm*100nm, the space between the contact and electrode is 25nm, and the effective resistivity is 200 μΩ*cm. From these figures, one can see that the size of an effective magnetoresistive element is around1.2 times of the size of a contact. Fig. 6A and 6B show the voltage potential and current density distribution for one CPP cell after considering of the effect of neighbor contacts. Here, the space is 50nm. The neighbor contacts has very limited effect on the size of effective magnetoresistive elements and shunting effect. Generally, the size of effective magnetoresistive elements reduces as the space reduces. Fig. 7 shows the conductance dependence on the memory block width with different thickness. The conductance of an effective magnetoresistive element of 2 micron is about 1.4 times of a patterned magnetoresistive element of the same size. The extra conductance is the result from the shunting effect of the effective magnetoresistive element in the memory block. In order to read the recorded signal, a current pulse can be applied to a digital line to switch the free layer of the memory block. As the coercivity of the memory block is much smaller than that of a patterned magnetoresistive element, the read power decreases.

Fig. 8A and 8B show the experimental result of the magnetoresistance curve of a MRAM device according to one embodiment of the present invention. The X-axis represents the external field H (Oe) and the Y-axis represents the magnetic resistance R (ohm or Ω). Fig. 8C and 8D show the magnetization states for an effective magnetoresistive element after thermal assistant writing. When a current pulse 938 is applied through a contact 934 and passes through a free layer 932, a space layer 937, and a recording layer 931, the temperature of an active area increases to near or over the Blocking temperature of the effective magnetoresistive element. A coincident positive magnetic field generated from the digital current can easily switch the magnetization 936 of the recording layer 931. After that, the pulse current 938 is removed, and the effective magnetoresistive element cools down. Even if there is no external field, the magnetization state 936 can be maintained as

shown in Fig. 8C. Similarly, the magnetization state 947 can be maintained after applying current pulse and a negative external magnetic field as shown in Fig. 8D. The recording and reading technique described in the present invention can also be used to record and read a spin-inject CPP MRAM and programmable metallization cell (PMC) memory. The thermal assistant writing is not required in the spin-inject MRAM and PMC memory.

Whilst the present invention has been described with reference to preferred embodiments it should be appreciated that modifications and improvements may be made to the invention without departing from the spirit and scope of the invention as defined in the following claims.

**WHAT IS CLAIMED:**

1. A magnetoresistive random access memory (MRAM) comprising:

a substrate;

a plurality of transistors formed on said substrate;

a plurality of memory blocks, each of said plurality of memory blocks having a recording layer and a plurality of active areas associated therewith; and

a plurality of contacts, each of said plurality of contacts couples an electrode of each of said plurality of transistors to an active area of each of said plurality of memory blocks,

wherein each of said plurality of transistors is controllable to activate a respective contact and thereby write onto said recording layer at a respective active area.

2. The MRAM as claimed in Claim 1, wherein said electrode of each of said plurality of transistors is a source of each of said plurality of transistors.

## ABSTRACT

**Nano-contacted magnetic memory device and method for making same**

A magnetic memory device comprising a plurality of switch transistors formed on a substrate; a plurality of magnetic memory blocks formed above the transistors; the plurality memory block is connected with the source or drain of the plurality of transistor through a plurality of contacts at respective active areas;. Large digital line is located above the memory blocks. Each memory block having many effective magnetoresistive elements that comprises a recording layer, a non-magnetic layer, and a free magnetic layer. Wherein the recording layer can be a synthetic-anti-ferromagnetic-pinned (SAFP) multi-layer, a ferri-magnetic layer, or a ferromagnetic layer. The magnetization of the recording layer at the active areas can be changed by a heating process and applying an external field induced from the digital line and the bit line or word line. The change in resistance of the effective magnetoresistive element can be detected by means of changing the magnetization of the free layer during reading. The magnetization of the whole memory block is changed during reading, thus a smaller switching field is required compare with conventional MRAM.

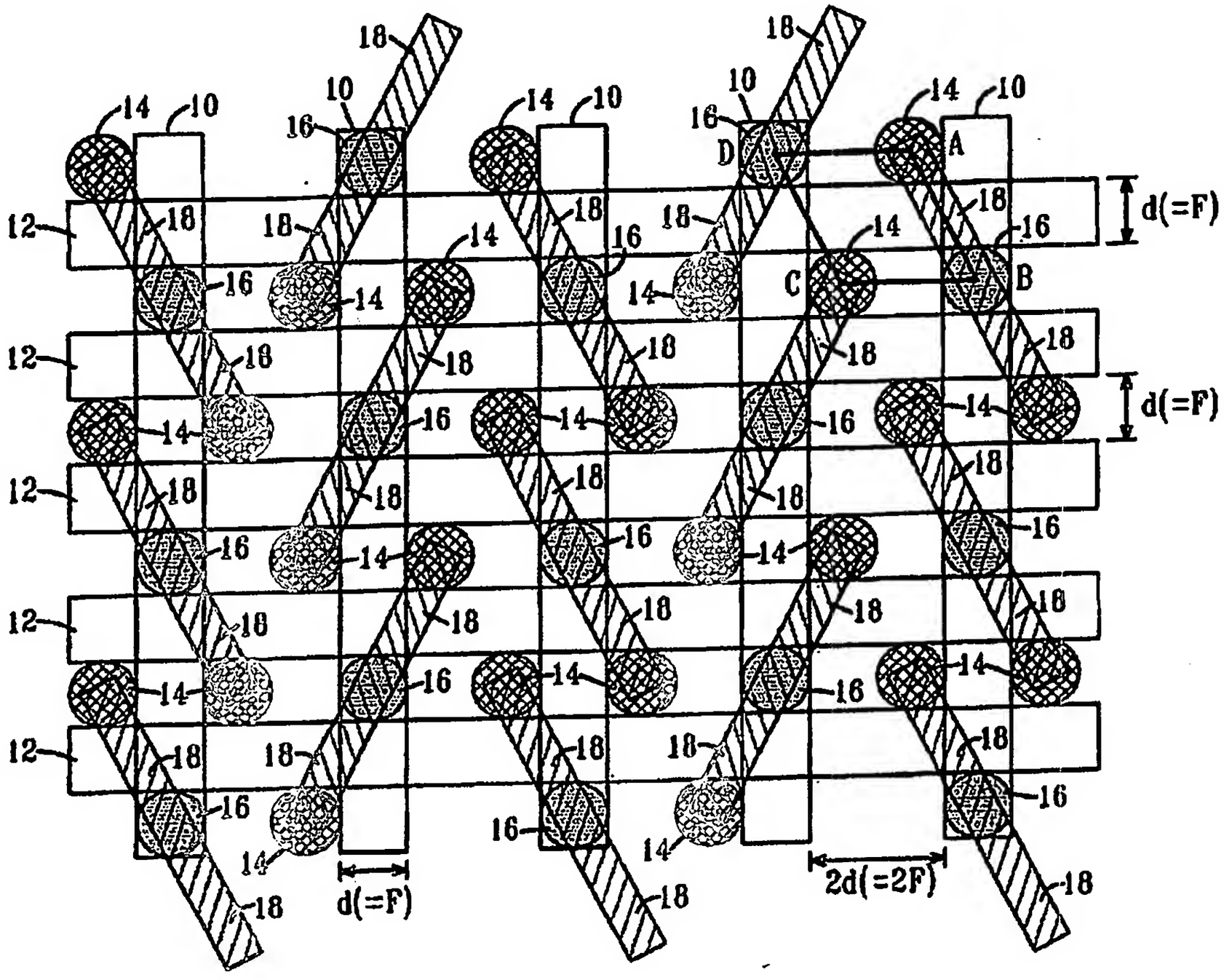


FIG. 1A

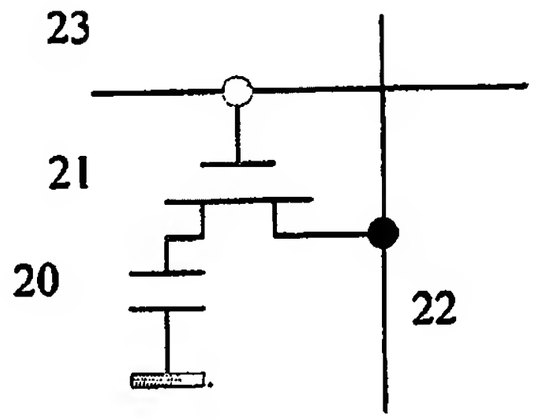


FIG. 1B

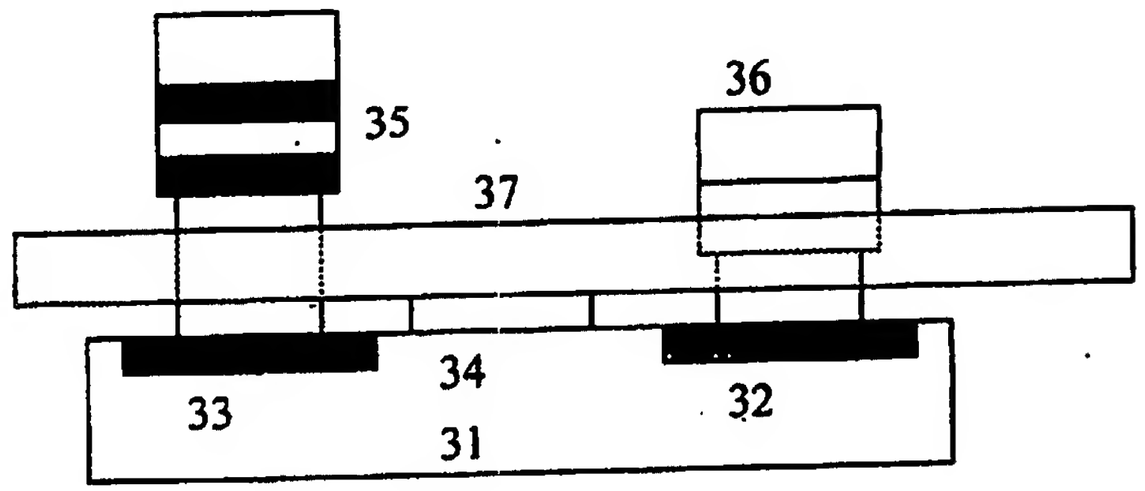


FIG. 1C

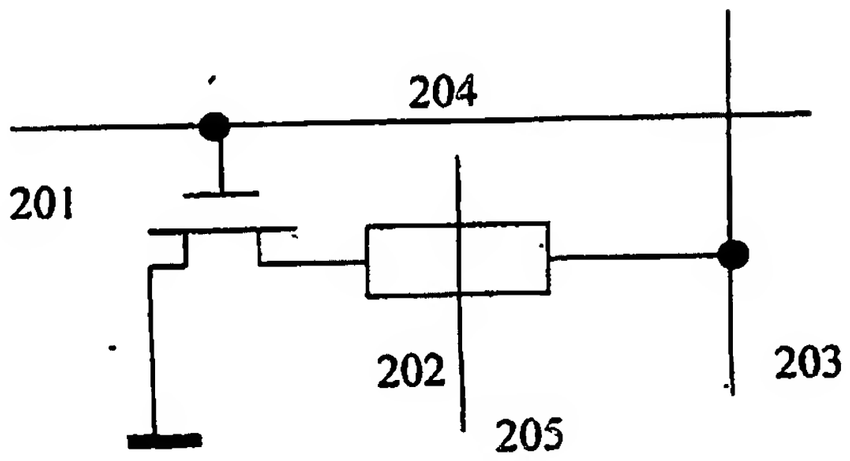


FIG. 2A

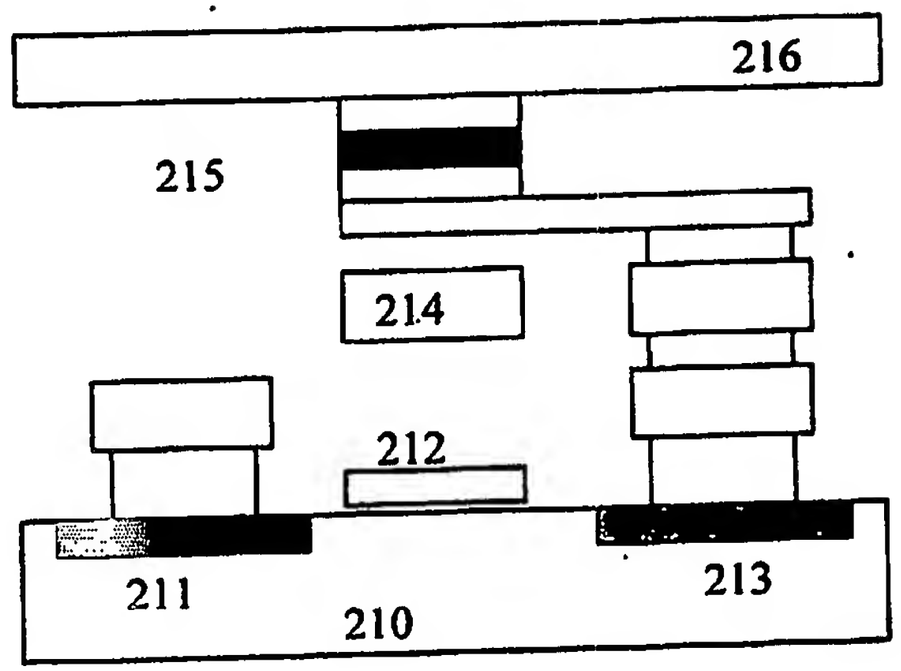


FIG. 2B

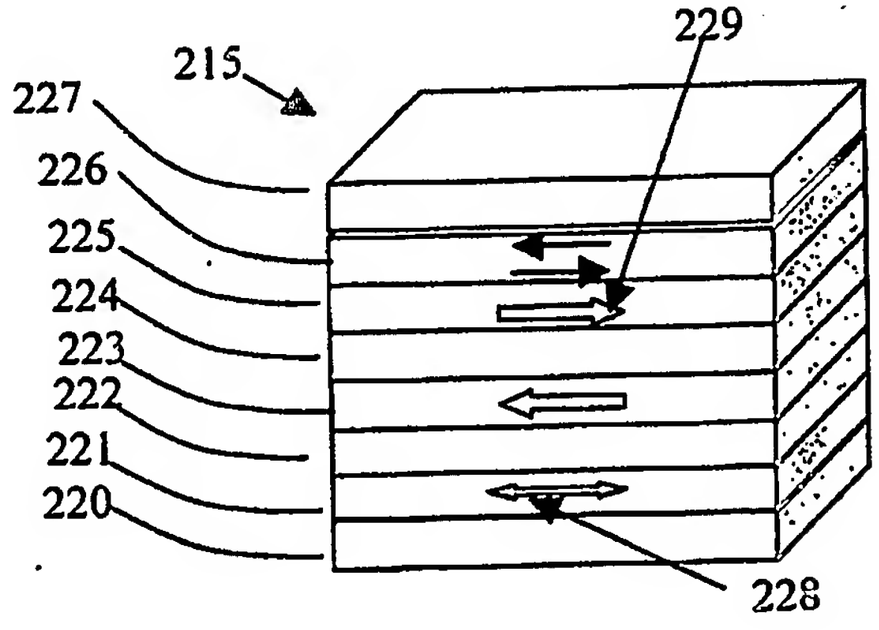


FIG. 2C

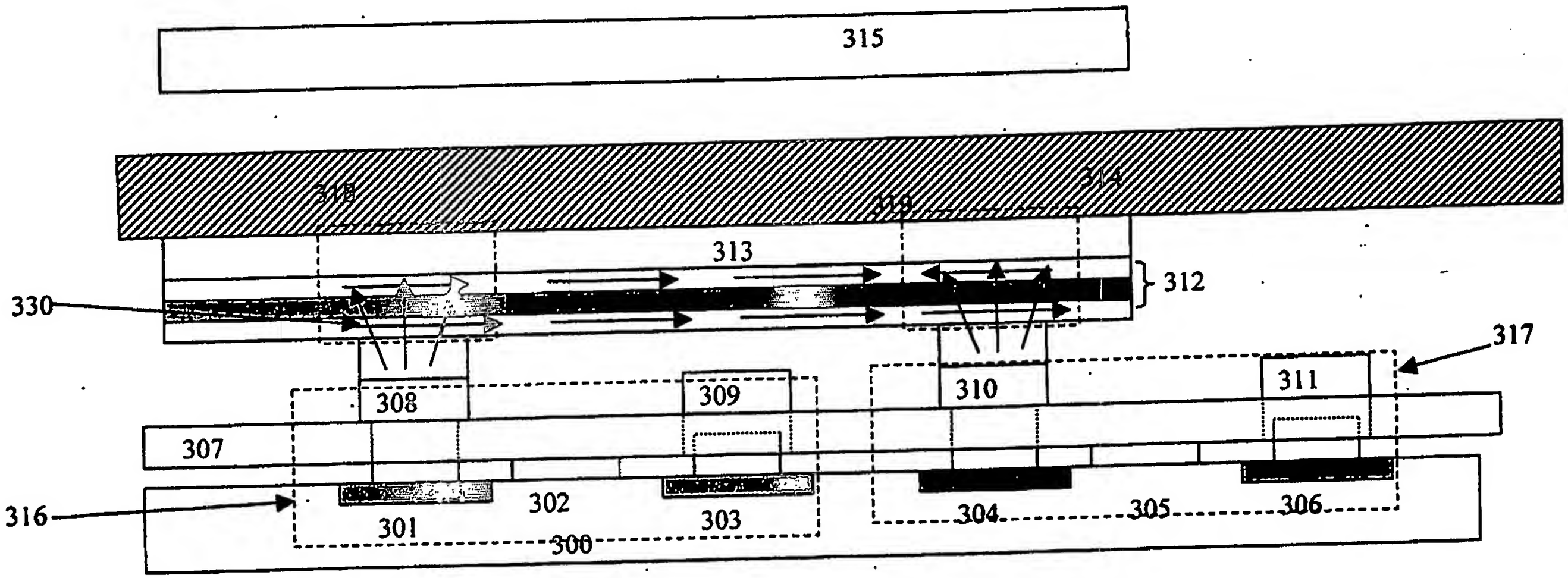
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FIG. 3A

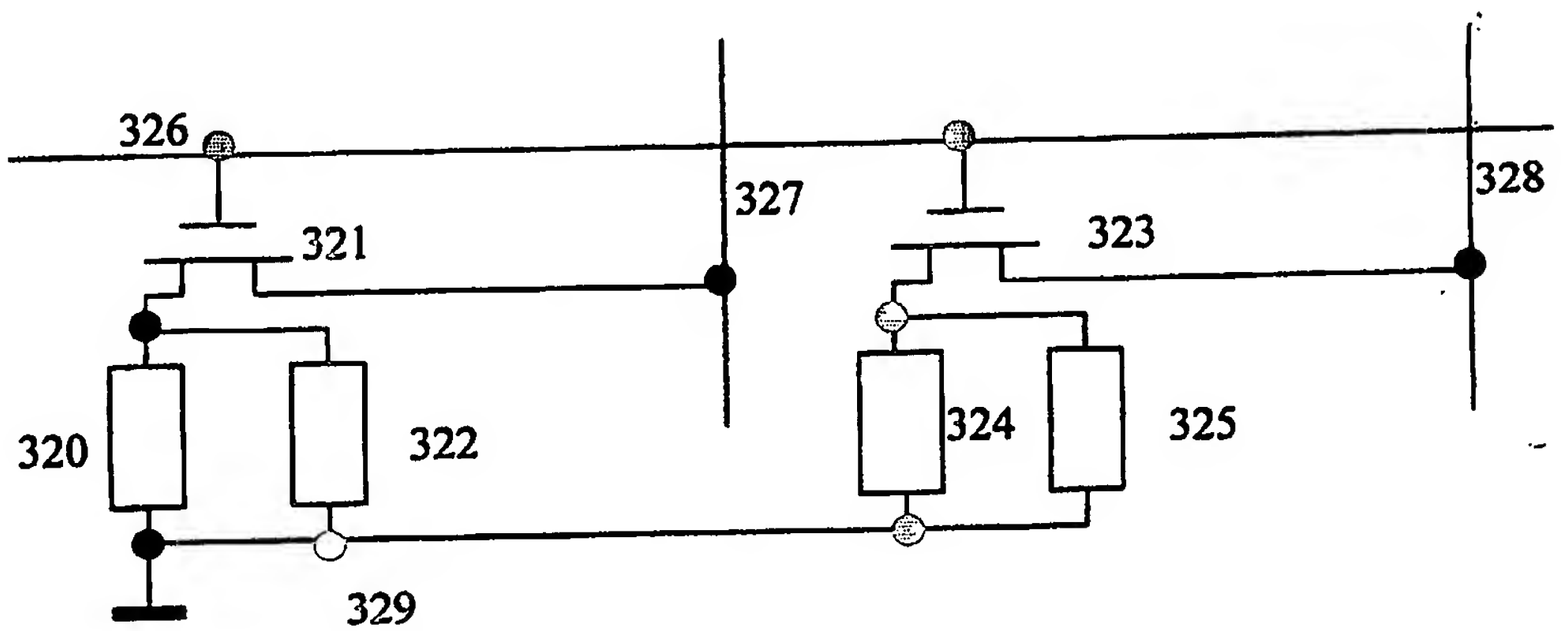



FIG. 3B

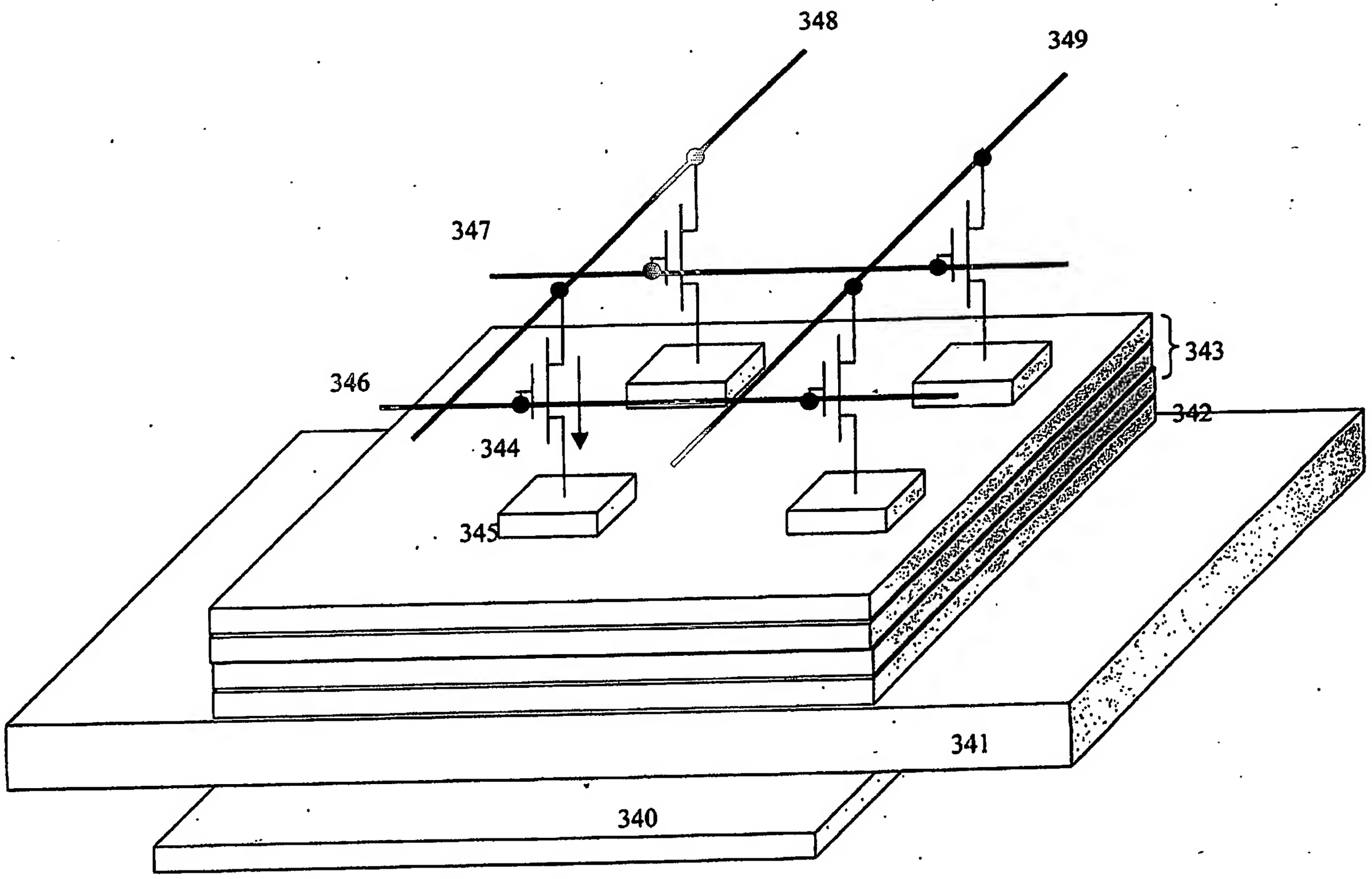
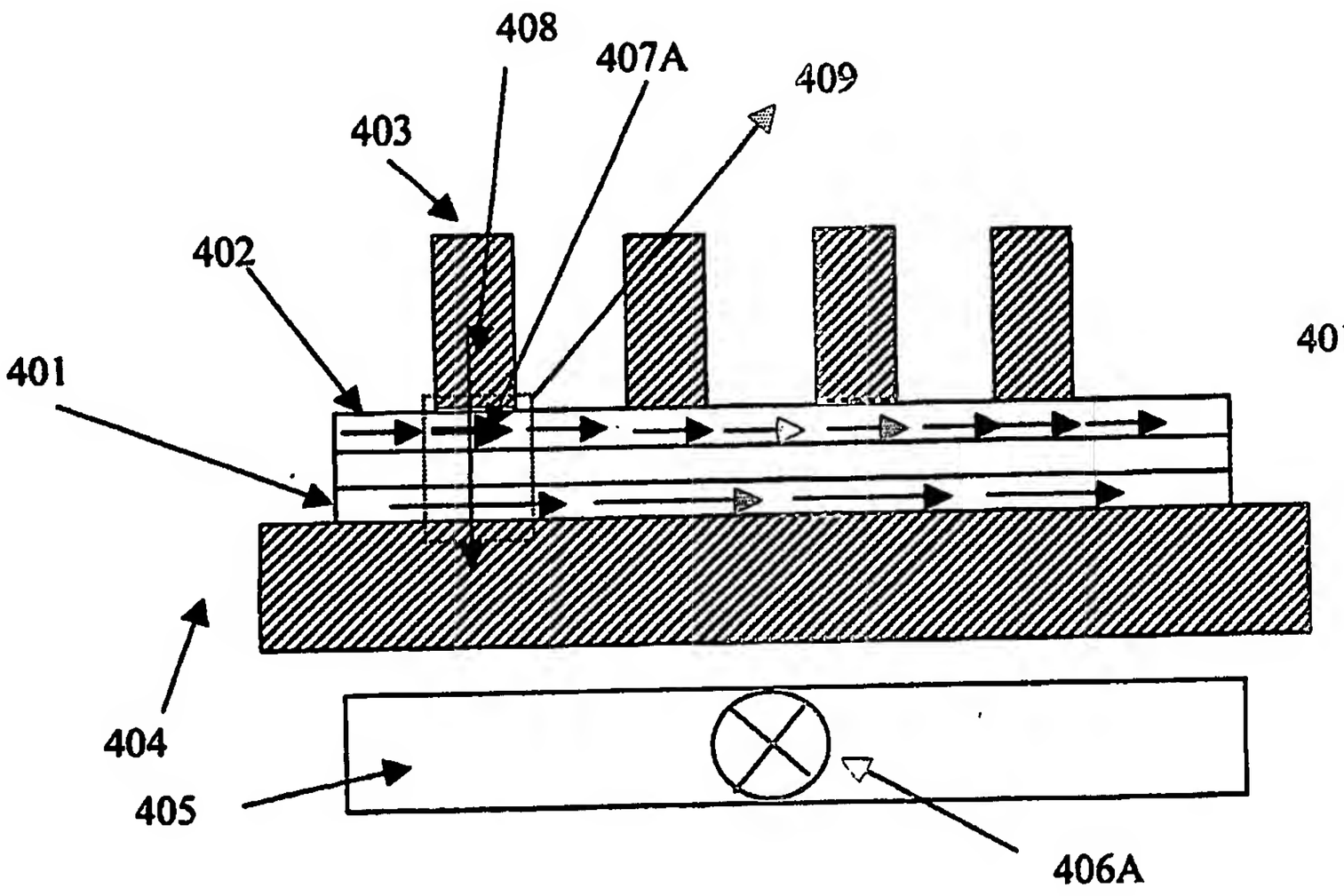



FIG. 3C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406A

FIG. 4A

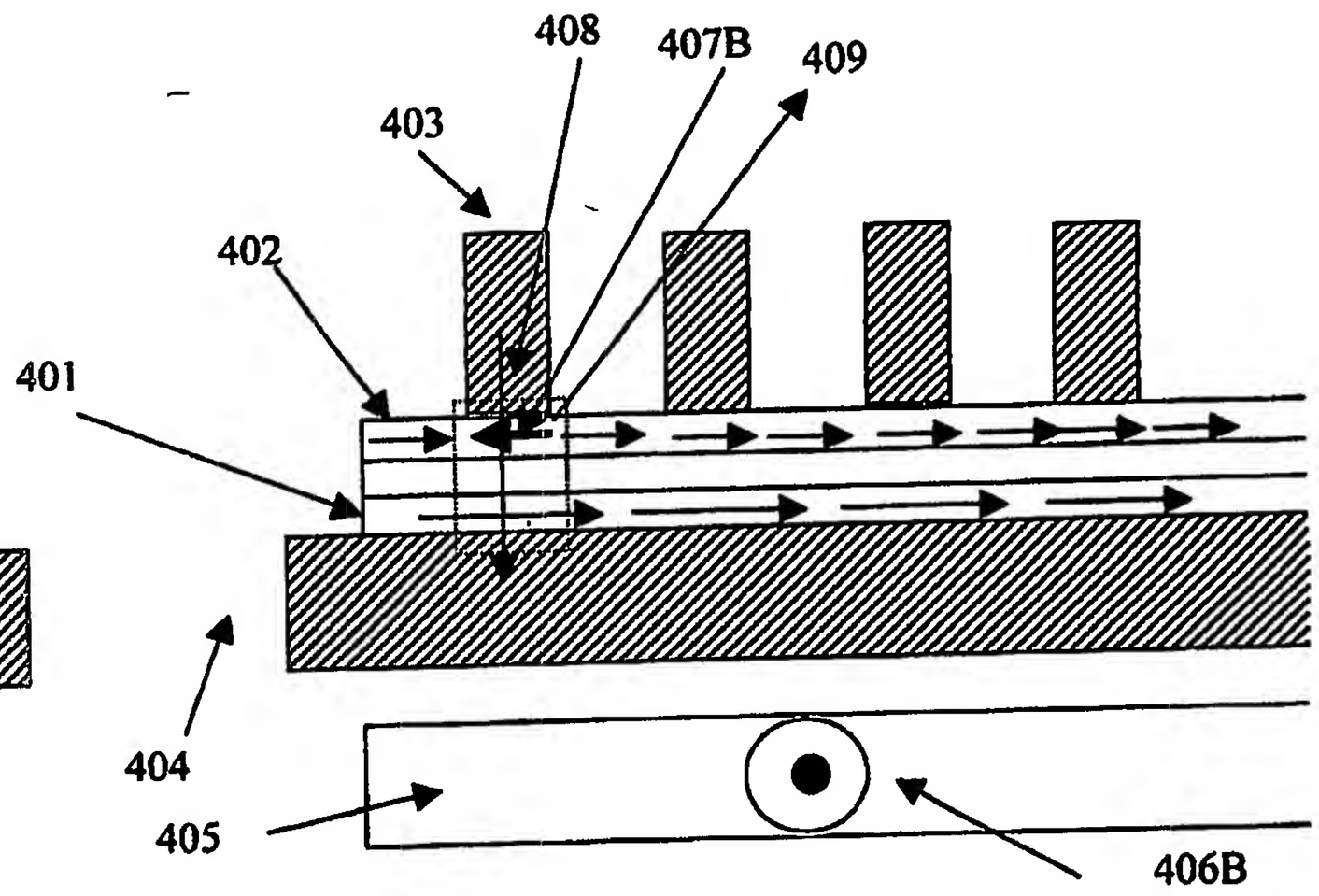
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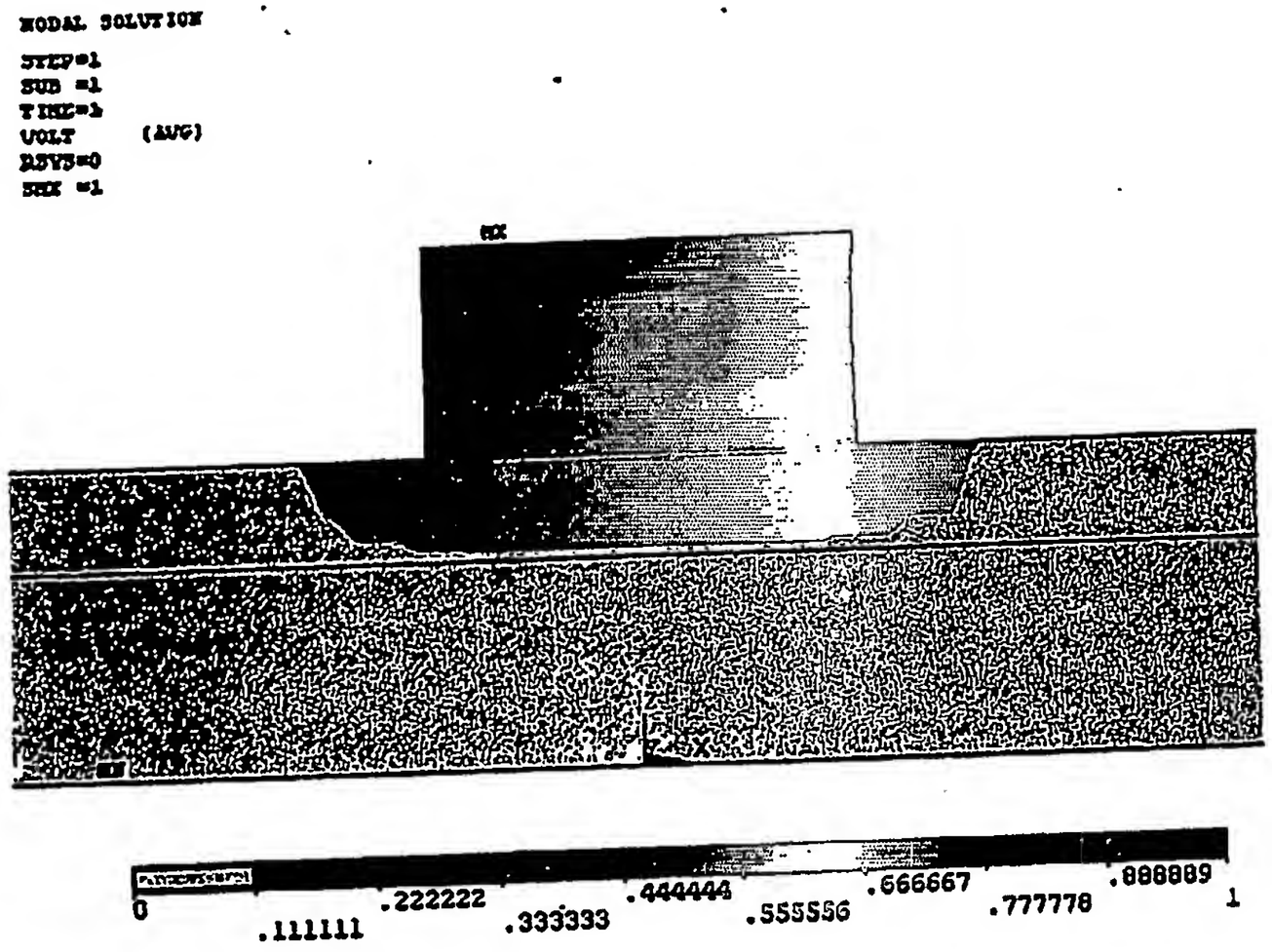
FIG. 4B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1

FIG.5A

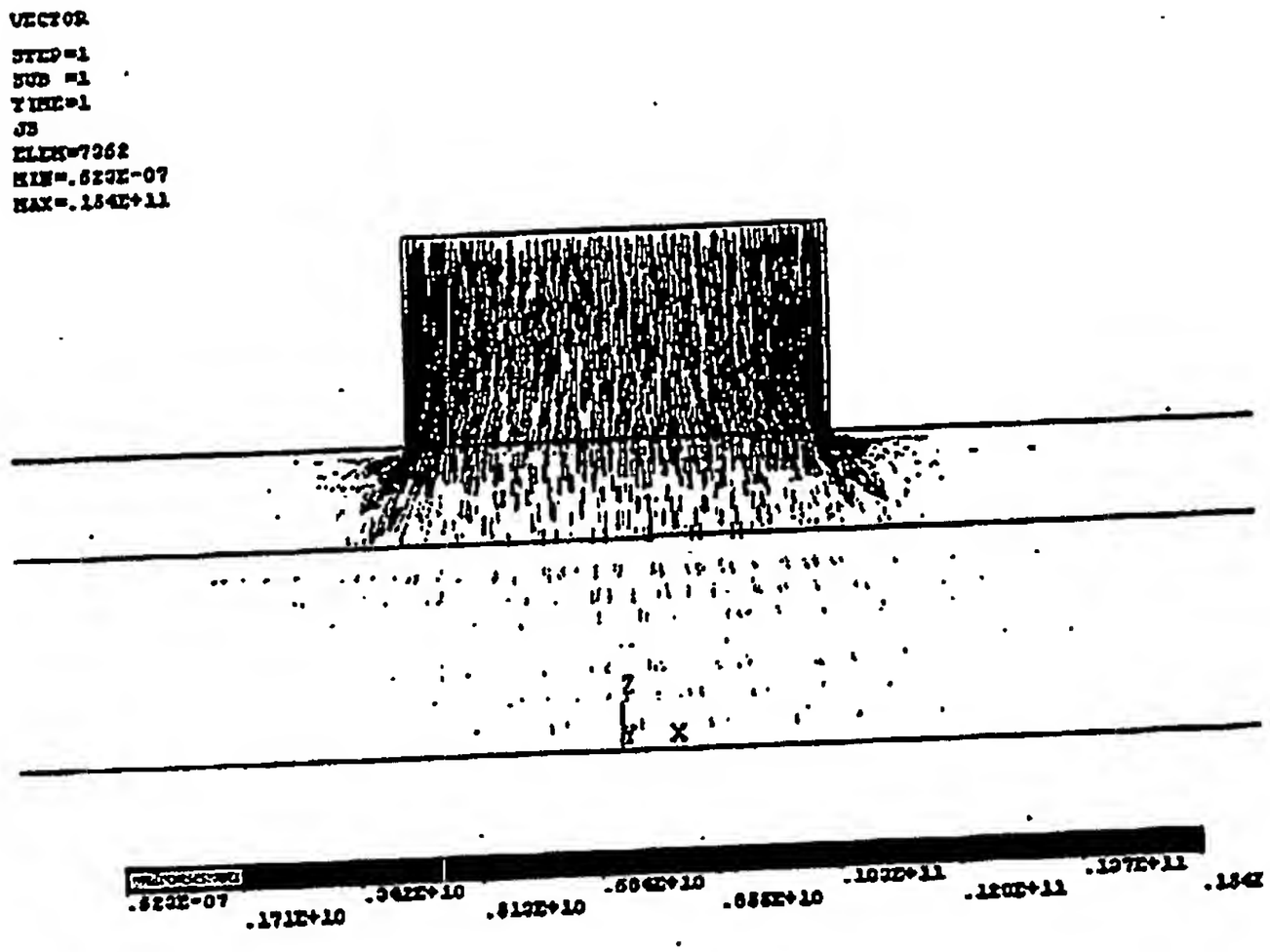
VECTOR
STEP=1
SUB =1
TIME=1
JS
ELEM=7362
MIN=.622E-07
MAX=.154E+11
Z
X
.622E-07
.171E+10
.342E+10
.513E+10
.684E+10
.855E+10
.103E+11
.120E+11
.137E+11
.154E

FIG.5B

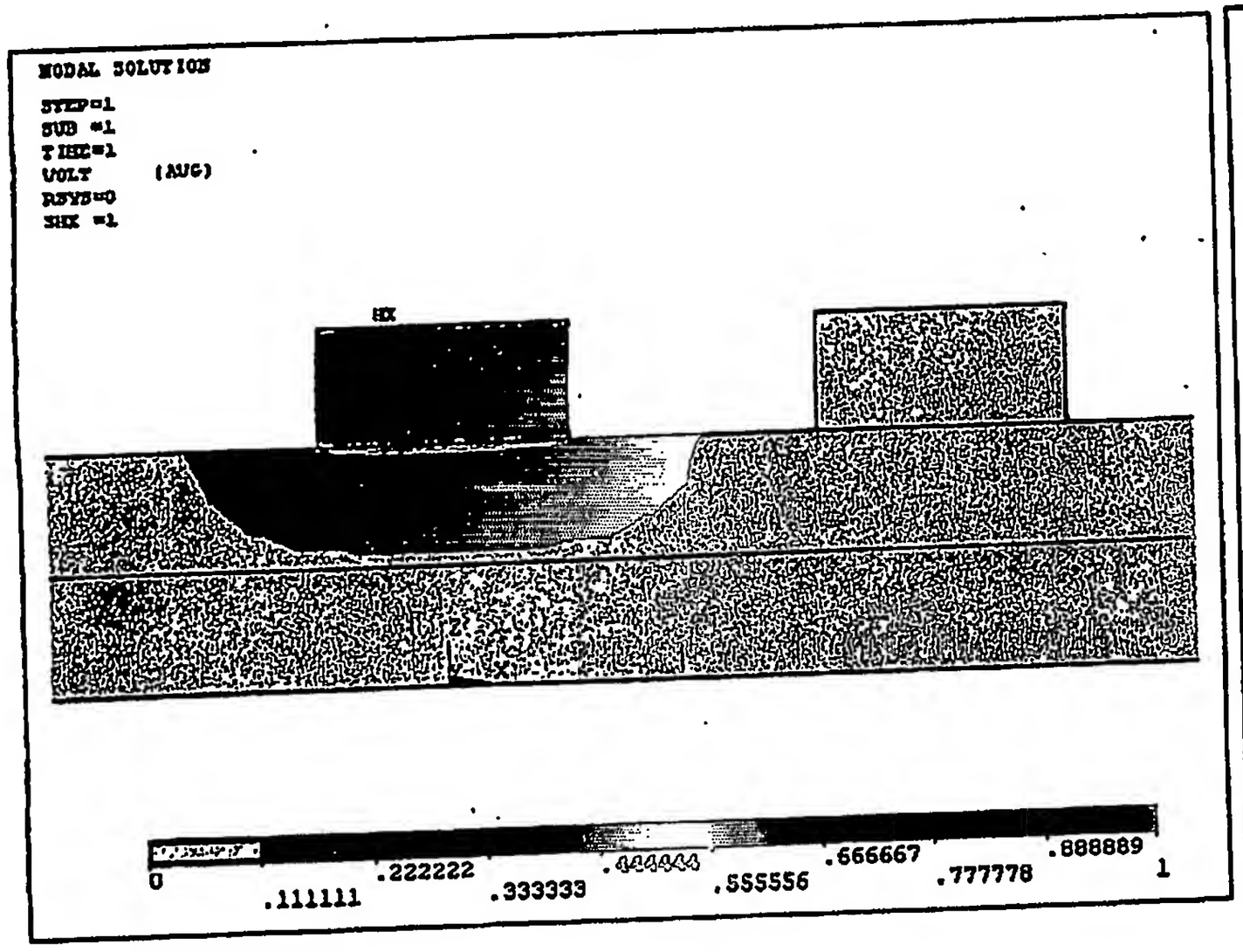
NODAL SOLUTION
STEP=1
SUB =1
TIME=1
VOLT (AVG)
RSYS=0
SHX =1
SHX
0
.111111
.222222
.333333
.444444
.555556
.666667
.777778
.888889
1

FIG.6A

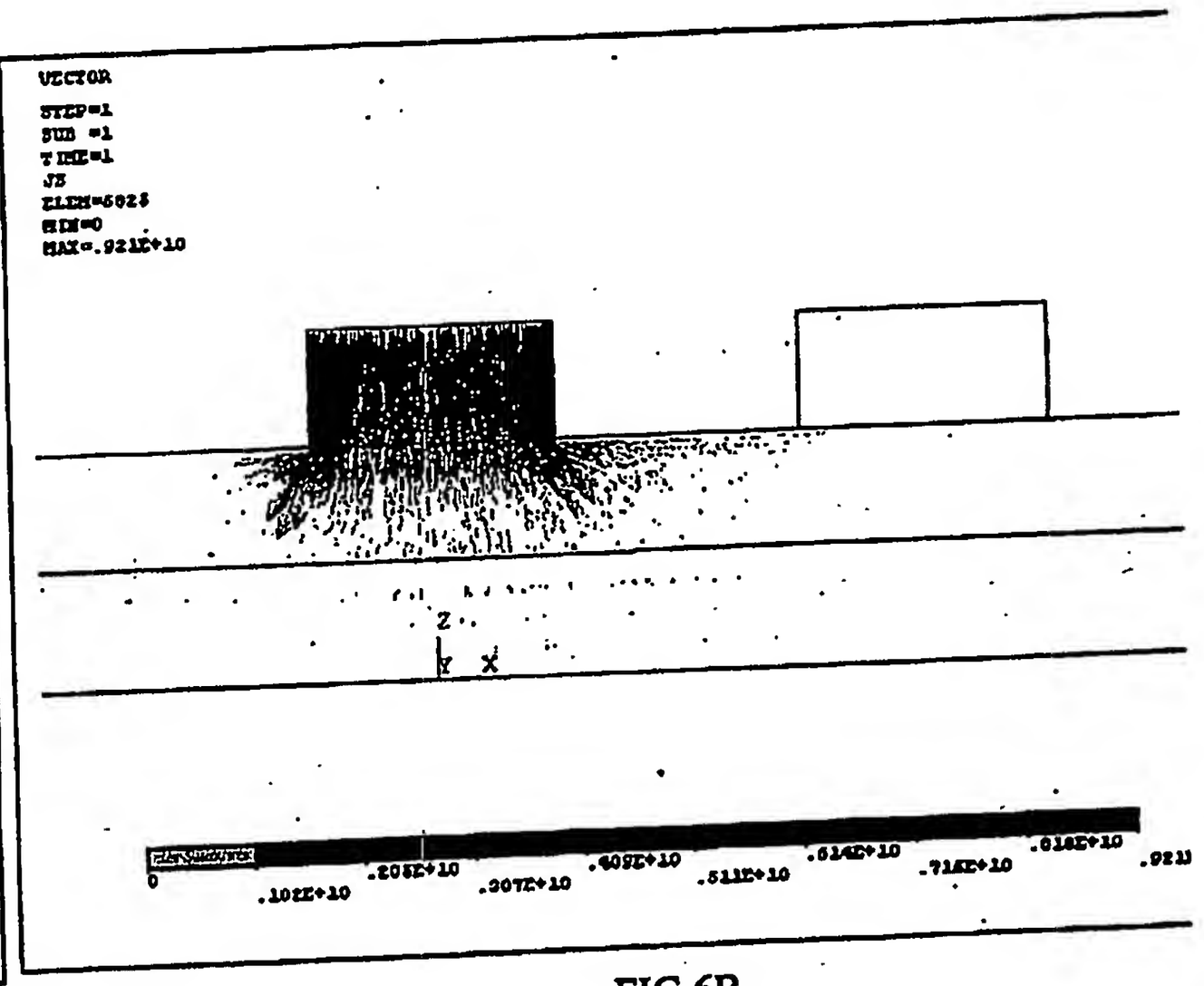
VECTOR
STEP=1
SUB =1
TIME=1
JS
ELEM=6028
MIN=0
MAX=.921E+10
Z
X
0
.102E+10
.205E+10
.307E+10
.409E+10
.511E+10
.614E+10
.716E+10
.818E+10
.921

FIG.6B

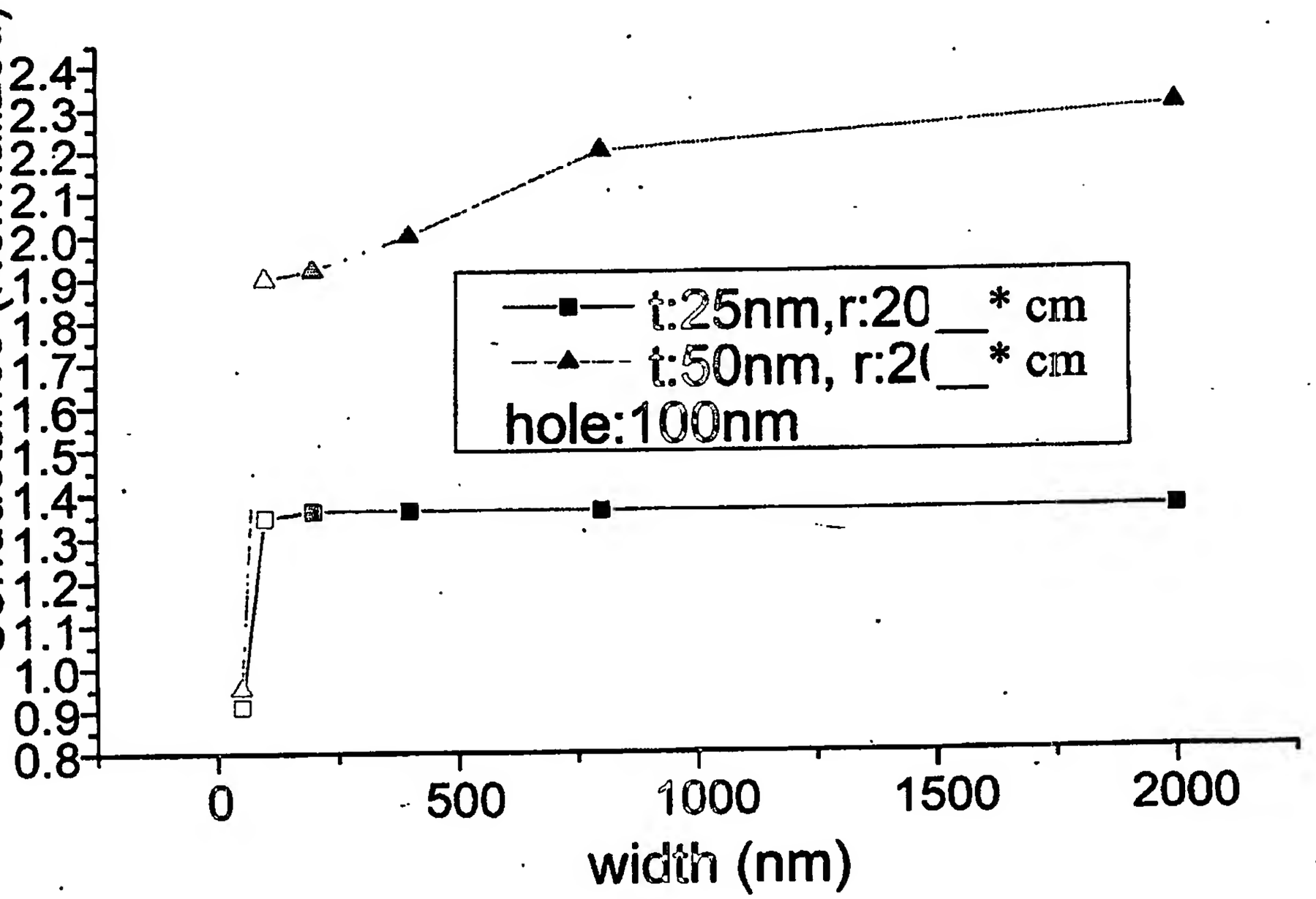
Conductance (Normalized)
2.4
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0
500
1000
1500
2000
width (nm)
t:25nm,r:20__* cm
t:50nm, r:2(__* cm
hole:100nm

FIG. 7

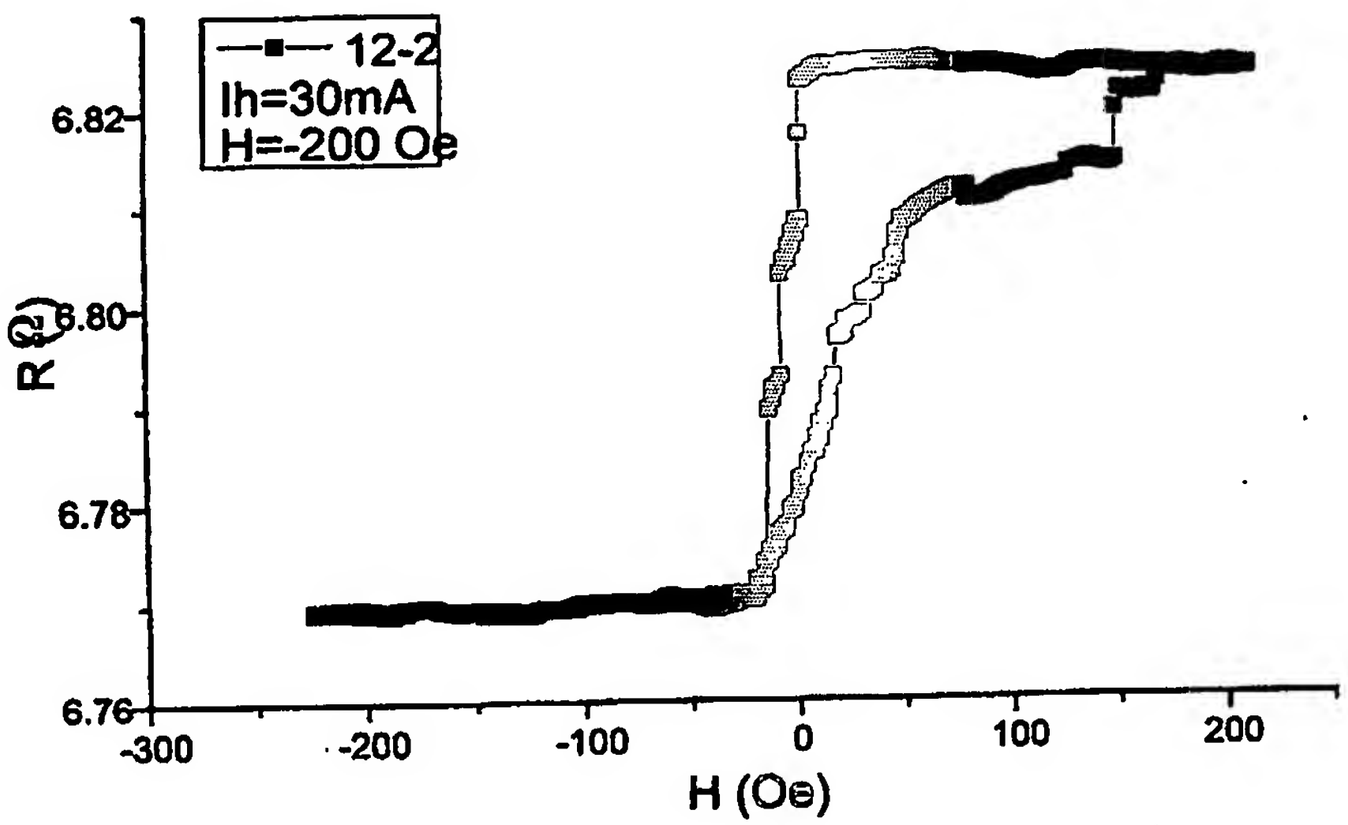
12-2
Ih=30mA
H=-200 Oe
R(Ω)
6.82
6.80
6.78
6.76
-300
-200
-100
0
100
200
H (Oe)

FIG. 8A

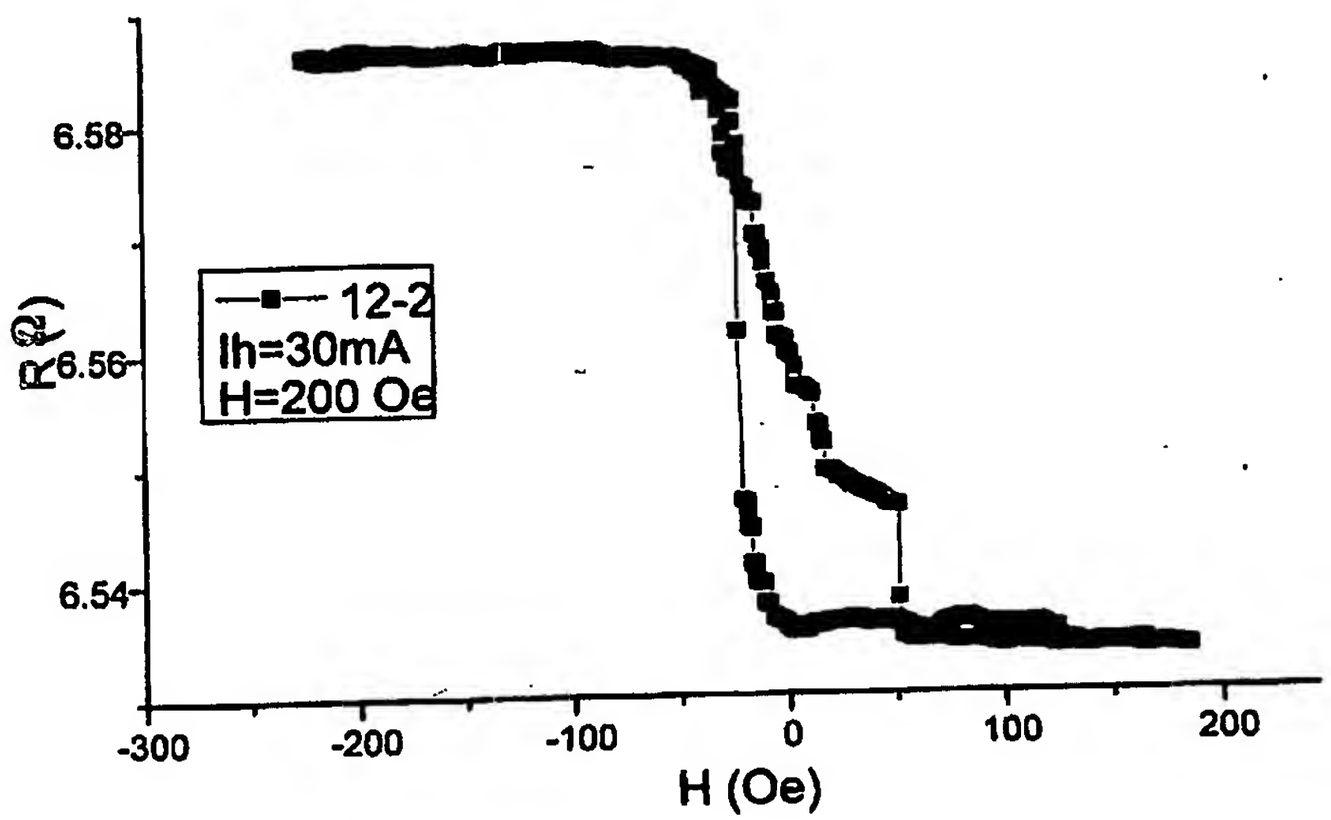
12-2
Ih=30mA
H=200 Oe
R(Ω)
6.58
6.56
6.54
-300
-200
-100
0
100
200
H (Oe)

FIG. 8B

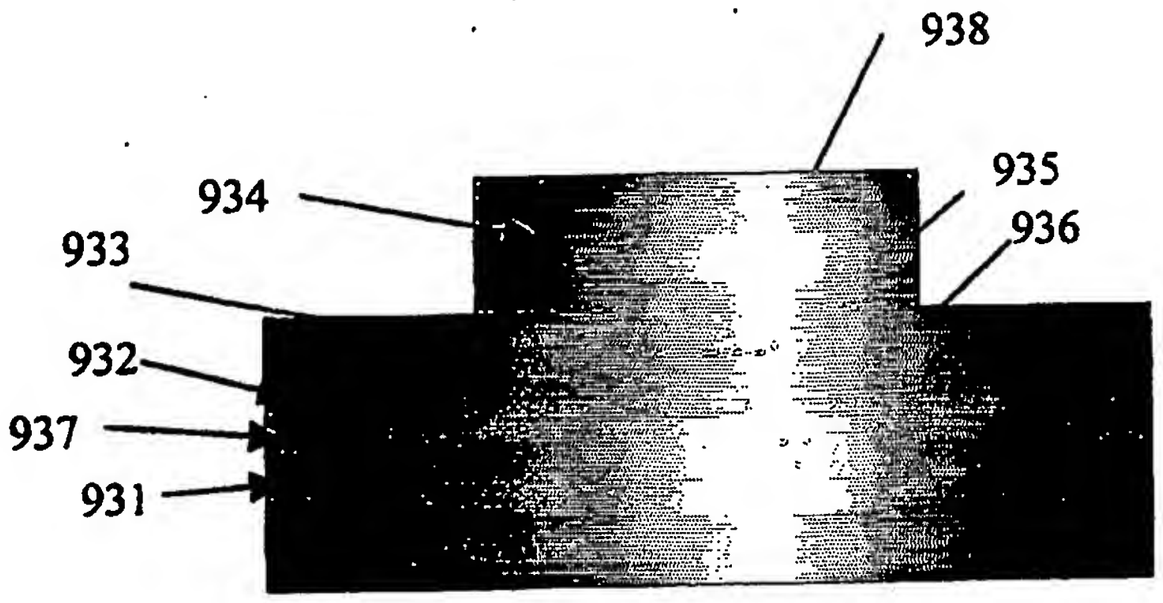


FIG. 8C

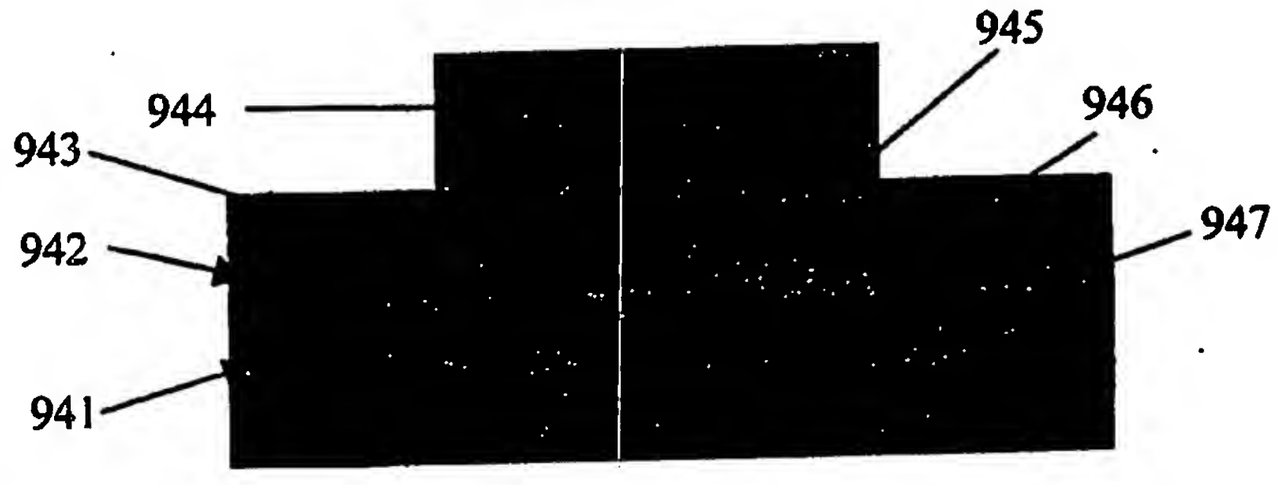


FIG. 8D